Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor position-sensitive radiation detection device, comprising:

a substrate formed of a semiconductor material doped to exhibit a first conductivity type and configured to have first and second surfaces opposing each other, the substrate having a bias layer proximate to the first surface and electrically coupled to the substrate, and an array of doped gate regions of a second conductivity type proximate to the second surface; and

a grid of conducting wires, formed of a first set of wires extending in a first direction, and a second set of wires extending substantially orthogonal to said first set of wires, proximate to and in electrical contact with the bias layer, ~~and configured to define~~ said grid surrounding a plurality of areas, each area surrounded by said grid forming a pixel, to form an array of pixels corresponding to the array of doped gate regions~~,~~

~~wherein the grid of conducting wires is configured to be electrically coupled to a voltage source and to distribute a bias voltage on the bias layer so as to bias the substrate with respect to the doped gate regions~~.

2. (Previously Presented) The device as in claim 1, wherein the bias layer comprises a region of the substrate proximate to the first surface that is more heavily doped with material of the first conductivity type than other regions of the substrate.

3. (Previously Presented) The device as in claim 1, wherein the bias layer comprises a transparent, conductive layer formed proximate to the first surface.

4. (Previously Presented) The device as in claim 3, wherein the bias layer includes a heavily-doped polycrystalline layer of the semiconductor material.

5. (Previously Presented) The device as in claim 1, wherein the bias layer includes a first transparent, conductive layer formed on the first surface and a second layer comprising a region of the substrate proximate to the first surface that is more heavily doped with a material of the first conductivity type than other regions of the substrate.

6. (Previously Presented) The device as in claim 1, further comprising a circuit layer proximate to the second surface and configured to provide a gate contact to and a readout circuit for each doped gate region.

7. (Currently Amended) The device as in claim 1, further comprising a scintillation array comprising plural scintillation elements at plural locations, each location of each scintillation element corresponding to one of said plurality of areas, said scintillation elements operable to convert incident radiation of a first wavelength outside a characteristic spectral response range of the substrate into secondary photons of a second wavelength within the characteristic spectral response range of the substrate, each of said scintillation elements aligned with and optically coupled to a corresponding one of the array of pixels, and wherein the scintillation array includes optically reflective surfaces disposed between the scintillation elements to optically isolate one scintillation element from another.

8. (Previously Presented) The device as in claim 7, wherein one of the first and second conductivity types is n-type and the other is p-type.

9. (Original) The device as in claim 7, wherein the substrate includes silicon.

10. (Previously Presented) The device as in claim 7, wherein the bias layer comprises a heavily-doped crystalline region of the substrate proximate to the first surface.

11. (Previously Presented) The device as in claim 7, wherein the grid of conducting wires comprises a metallic material.

12. (Original) The device as in claim 11, wherein the metallic material includes aluminum.

13. (Previously Presented) The device as in claim 7, further comprising an anti-reflection layer proximate to the bias layer within each pixel and configured to reduce reflection of photons incident on the first surface.

14. (Original) The device as in claim 13, wherein the anti-reflection layer is electrically insulating.

15. (Previously Presented) The device as in claim 13, wherein the anti-reflection layer includes a dielectric layer having a refractive index that has a relation with a refractive index of the bias layer.

16. (Previously Presented) The device as in claim 1, wherein one of the first and second conductivity types is n-type and the other is p-type.

17. (Original) The device as in claim 1, wherein the substrate includes silicon.

18. (Previously Presented) The device as in claim 7, further comprising an anti-reflection layer proximate to the bias layer within each pixel and configured to reduce reflection of photons incident on the first surface.

19. (Currently Amended) A semiconductor position-sensitive radiation detection device, comprising:

~~an array of photodiodes formed in~~ a substrate having a first surface and a second surface opposing the first surface[[,]];

a plurality of photodiodes formed in said substrate in rows and columns defining an array; ~~wherein~~

a bias layer, proximate to the first surface [[is]] and electrically conducting to provide a common bias potential to each of the photodiodes and [[is]] optically transparent to receive input photons to be detected; and

a grid of conducting wires proximate to and in electrical contact with the bias layer and configured to ~~define an array of~~ surround each of the pixels ~~corresponding to~~ of the array of photodiodes~~, wherein the grid of conducting wires is further configured to distribute a common potential to the photodiodes~~.

20. (Previously Presented) The device as in claim 19, further comprising a scintillation array of scintillation elements operable to convert incident radiation at a first wavelength outside a characteristic spectral response range of the photodiodes into secondary photons at a second wavelength within the characteristic spectral response range of the substrate and coupled to the grid of conducting wires proximate to the bias layer, each of said scintillation elements aligned with and optically coupled to a corresponding one of the array of pixels, and wherein the scintillation array includes optically reflective surfaces disposed between the scintillation

elements to optically isolate one scintillation element from another.

21. (Prevously Presented) The device as in claim 20, further incorporating an anti-reflection layer proximate to the bias layer within each pixel and configured to reduce reflection of photons incident to the first surface.

22. (Original) The device as in claim 21, wherein the anti-reflection layer is electrically insulating.

23. (Original) The device as in claim 21, wherein the anti-reflection layer includes a dielectric layer having a refractive index that has a relation with a refractive index of the first surface.

24. (Previously Presented) The device as in claim 19, further incorporating an anti-reflection layer proximate to the bias layer within each pixel and configured to reduce reflection of photons incident to the first surface.

25. (Previously Presented) The device as in claim 19, further comprising a circuit layer proximate to the second

surface and configured to provide electrical contact with said array of photodiodes.

26. (Previously Presented) The device as in claim 19, wherein the substrate is doped to exhibit a first conductivity type, and wherein the bias layer comprises a region of the substrate proximate to the first surface, where the region is more heavily doped with a material of the first conductivity type than the rest of the substrate.

27. (Previously Presented) The device as in claim 19, wherein the bias layer comprises a transparent conductor layer formed proximate to the first surface.

28. (Previously Presented) The device as in claim 27, wherein the substrate comprises a semiconductor material, and wherein the transparent conductor layer includes a heavily-doped polycrystalline layer of the semiconductor material.

29. (Previously Presented) The device as in claim 1, wherein the bias layer is a conducting bias electrode layer.

30. (Previously Presented) The device as in claim 1, wherein the bias layer is a back contact layer.

31. (New) A device as in claim 1, further comprising a connection to said grid of conducting wires, which provides a bias voltage across said grid of conducting wires.

32. (New) A device as in claim 1, further comprising means, coupled to said grid of conducting wires, for distributing the bias voltage on the bias layer to bias the substrate with respect to the doped gate regions.

33. (New) The device as in claim 1, wherein said bias layer is a separate layer which is attached to said substrate.

34. (New) The device as in claim 1, wherein said bias layer is a portion of said substrate which has been changed in characteristics.

35. (New) The device as in claim 7, wherein said scintillation array comprises a plurality of trenches, formed in the substrate, extending part way through the substrate, and

said optically reflective surfaces comprise a reflective material filled into the trench.

36. (New) The device as in claim 7, wherein said scintillation array comprises a plurality of trenches, formed in said substrate, extending part way through the substrate, and said optically reflective surfaces comprise a reflective material covering sidewalls of the trenches.

37. (New) The device as in claim 13, wherein the anti-reflection layer comprises a plurality of dielectric layers forming a metallic material.

38. (New) The device as in claim 13, wherein said grid of conducting wires is formed to be substantially coplanar with said anti-reflection layer.

39. (New) A device as in claim 19, further comprising an anti-reflection coating, proximate to an electrical contact with the bias layer, and substantially coplanar with said grid of conducting wires.

40. (New) A device as in claim 20, wherein said scintillation array is formed of a semiconductor substrate with trenches in said substrate, said trenches being substantially aligned with said grid of conducting wires.

41. (New) A device, comprising:

a semiconductor substrate having first and second opposing surfaces;

a plurality of doped regions within said semiconductor substrate proximate to said first surface, forming gates within said semiconductor substrate, said gates formed in a regular pattern defining an array;

a transparent bias layer, proximate to said second surface;

an array of conducting wires, forming a two-dimensional grid with a first plurality of parallel wires extending in a first direction, and a second plurality of parallel wires extending in a second orthogonal direction to said first direction, said first and second plurality of wires in electrical contact with one another at each of a plurality of contact locations, and defining a plurality of substantially rectangular areas defining a perimeter, wherein each perimeter formed by each of said substantially rectangular areas surrounding one of said gates and forming a pixel.

42. (New) A device as in claim 41, further comprising an anti-reflection coating, proximate to said second surface.

43. (New) A device as in claim 42, wherein said anti-reflection coating is substantially coplanar with said array of conducting wires.

44. (New) A device as in claim 42, wherein said anti-reflection coating is formed of a plurality of dielectric layers forming a dialectric stack.